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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/727,320	12/03/2003	Charles R. Lefurgy	AUS920030894JS1	6220

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EXAMINER	
SUGENT, JAMES F	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 04/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/727,320	LEFURGY ET AL.	
	Examiner	Art Unit	
	James Sugent	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03 December 2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 16-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Faucher et al. (U.S. Patent No. 5,404,543) (hereinafter referred to as Faucher).

As to claim 16, Faucher discloses a device controller (memory controller 20) for coupling (via bus 42) a group of devices (memory banks 30) to one or more processors (CPU 12) in a processing system, comprising: a command unit (system memory machine 60) for sending commands (RAS and CAS) to said one or more devices (via control bus 36; column 4, lines 25-40 and column 5, lines 54-66); at least one control register (70, 72 and 74 within scoreboard 64) for receiving a local maximum power consumption bound (Faucher discloses said scoreboard being updated with a base memory size to manage the amount of memory maintained to directly manage power with in the system; column 6, lines 16-20 and column 9, lines 10-31); and control logic (power management machine 66) coupled to said at least one control register (within scoreboard) and further coupled to an input of said command unit (Faucher discloses the command unit [system memory machine 60] accommodating various cycles in correlation with control logic [power management machine 66] which necessitates the coupling of these two to each other; column 5, lines 56-61) for sending power management commands (alters voltage

delivered to memory modules [30]) with maintaining a total power consumption of said group of devices below said local maximum bound (column 2, lines 25-35), whereby said device controller power manages said group of devices without intervention by said one or more processors (Faucher discloses a power saving method wherein if a memory module [30] has not been accessed within said pre-determined time period then the device controller [memory controller 20] and control logic [power management machine 66] place the memory bank [22] into a lower power mode; column 12, line 67 thru column 13, line 6 and column 13, line 67 thru column 14, line 21) .

As to claim 17, Faucher discloses the device controller further comprising at least one other control register (70, 72 or 74) for receiving a local minimum power bound (as discussed hereinabove), wherein said control logic is further coupled to said at least one other control register (70, 72 or 74) for sending power management commands consistent with maintaining a total power consumption of said group of devices above said local minimum bound, whereby changes in power consumption of each of said groups is limited to avoid excessive current spikes within a power distribution network of said processing system (Faucher discloses making the bank of memory within the system accessible dependent on the range defined and therefore power consumed; column 6, lines 15-55).

As to claim 18, Faucher discloses the device controller wherein said device controller is a memory controller (20), said devices are memory modules (30), and wherein said command unit sets a power management state of each associated memory module (column 5, lines 54-66).

As to claim 19, Faucher discloses the device controller further comprising evaluators (power management machine 66) for evaluating a usage of each associated device in order to

determine whether or not said usage of each device has fallen below a threshold (power utilization), and wherein said control logic further determines said power management settings for each particular device in conformity with said measured usage for each particular device (column 5, lines 13-24 and column 6, lines 10-15 and column 7, lines 38-58).

As to claim 20, Faucher discloses the device controller further comprising a storage (buffer 52) containing an access queue (stack, as is known in the art is a list of commands) for each of said associated devices, and wherein said control logic further determines said power management settings for each particular device in conformity with a number of accesses queued for each particular device (column 5, lines 13-32).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeddeloh et al. (U.S. Patent Publication No. 2004/0260957 A1) (hereinafter referred to as Jeddeloh) in view of Fung (U.S. Patent Publication No. 2002/0004913 A1) (hereinafter referred to as Fung) and Adachi (U.S. Patent No. 7,000,130 B2) (hereinafter referred to as Adachi).

As to claim 1, Jeddeloh discloses a method of managing power in a processing system, comprising: a plurality of groups of devices within said processing system (DRAM devices 104 within modules 504 and 508) wherein each group of devices has an associated device controller

(paragraphs 23, 36 and 39); a second determining power management states (Jeddeloh discloses a memory system wherein memory modules can be placed into a power saving mode, can be throttled or use another reduced power mode and thus has multiple power states; paragraph 15, lines 15-20) for each device within each of said groups of devices within said associated local controller (paragraph 23) consistent with said associated local maximum bound, whereby said global maximum power consumption bound ("average temperature level across the memory array"; paragraph 28) is met by meeting all of said local bounds (Jeddeloh discloses an average [global] temperature of the memory devices [104] being maintained based upon individual local thresholds; paragraphs 28 and 29); and, setting said power management state of each device from said associated local controller (Jeddeloh discloses the power controllers [360 or 520 and 524] determining and setting the power states; paragraphs 23 and 29).

Jeddeloh fails to disclose: determining an associated local maximum bound of power consumption for each of a plurality of groups of devices within said processing system wherein a sum of said local bounds is less than a global maximum power consumption bound for said processing system; and, communicating each local maximum bound to an associated one of a plurality of local controllers coupled to said associated group of devices.

Fung teaches a server rack (52) comprising one or two device controllers (management modules 53) that control and manage the power of multiple groups of devices (server modules 54) (paragraphs 40 and 43). Power management is inclusive of observing server module activity indicators and altering the power states if thresholds within the system are crossed both globally and locally (paragraphs 106-108) wherein said thresholds can be predetermined and set or dynamically (paragraphs 168 and 248) and said thresholds (bounds) are communicated to an

associated local controller coupled to said associated group of devices (Fung discloses new activity indicators generated are communicated to the memory of the server modules for use by the activity monitor; paragraph 104). Fung also has the added benefit of managing the overall computer system temperature using cooling fans (paragraph 42).

It would have been obvious to one of ordinary skill of the art having the teachings of Jeddeloh and Fung at the time the invention was made, to modify the device controllers of Jeddeloh to include the ability to dynamically alter activity thresholds as taught by Fung such that the power management scheme of Jeddeloh has the ability to alter thresholds dynamically and communicate new thresholds to the device controllers. One of ordinary skill in the art would be motivated to make this combination of having the ability to alter thresholds dynamically and communicate new thresholds to the device controllers in view of the teachings of Fung, as doing so would give the added benefit of managing the overall computer system temperature using cooling fans (paragraph 42).

Adachi teaches method and apparatus for power saving using clock throttling within an integrated circuit (201) using a device controller (controlled clock generator 202) that collects activity information of a plurality (205, 207 and 209) of groups of devices (functional blocks unit0, unit1, unit2, unit3, unit4, unit5 and unit6) (column 3, lines 43-55) and alters the clock of said devices (column 2, lines 35-4) such that the total of the local bounds (thresholds) is less than a global power consumption bound (measure of global activity) for said processing system (Adachi teaches an activity monitoring technique wherein the sum of the local activity indicators are less than a global threshold such that the total of the local indicators is capable of exceeding

the global level; column 9, lines 35-56). Adachi has the added benefit of providing a safe clock throttling technique to that prevents current spikes within the system (column 2, lines 21-34).

It would have been obvious to one of ordinary skill of the art having the teachings of Jeddeloh, Fung and Adachi at the time the invention was made, to modify threshold mechanisms of Jeddeloh to include the sums of the local threshold indicators is less than a global threshold as taught by Adachi. One of ordinary skill in the art would be motivated to make this combination of ensuring that the global threshold is less than the sum of local threshold in view of the teachings of Adachi, as doing so would give the added benefit of providing a safe clock throttling technique to that prevents current spikes within the system (column 2, lines 21-34).

As to claim 2, Jeddeloh discloses the method wherein said local controllers are memory controllers (360), said devices are memory modules (104), and wherein said setting sets a power management state of each of said memory modules from an associated memory controller (Though Jeddeloh discloses the controllers are within the memory modules and the devices are arrays of DRAM memory it would be known in the art that the same scope can be applied to memory modules and memory controllers; paragraphs 23-24 and 28-29).

As to claim 3, Jeddeloh discloses the method further comprising evaluating a usage of each of said devices by said device controller in order to determine whether or not said usage of each device has fallen below a threshold, and wherein said second determining determines said power management settings for each particular device in conformity with said measured usage for each particular device (paragraphs 23-24 and 28-29).

As to claim 4, Jeddeloh discloses the method wherein each of said local controllers includes a storage containing an access queue for each of said associated devices, and wherein

said second determining determines said power management settings for each particular device in conformity with a number of accesses queued for each particular device (Jeddeloh discloses responding to a reduction in response time in a memory module dependent on the number commands received which, as is known in the art, is received within a buffer in the system; paragraph 14).

As to claim 5, Jeddeloh discloses the method wherein said processing system includes multiple processing locales (104), wherein each of said local controllers is a power management controller for an associated processing locale, whereby said second determining and said setting control the power consumption of each of said multiple processing locales in accordance with meeting said global maximum power consumption bound (paragraphs 28 and 29).

As to claim 6, Jeddeloh discloses the method wherein said setting sets power management states of said processing locales (104) including a shutdown state of said processing locales (paragraphs 23-24 and 28-29).

As to claim 7, Fung teaches the method further comprising: third determining an associated local minimum bound of power consumption for each of a plurality of groups of devices within said processing system (paragraphs 168 and 248); and communicating each local minimum bound to an associated one of a plurality of local controllers coupled to said associated group of devices (paragraph 104).

Jeddeloh discloses the method further comprising: wherein said second determining further determines power management states for each device within each of said groups of devices within said associated local controller consistent with said associated local minimum bound, whereby changes in power consumption of each of said groups is limited to avoid

excessive current spikes within a power distribution network of said processing system (Jeddeloh discloses activity indicators reaching a certain threshold and falling below a certain threshold; paragraphs 23-24 and 28-29).

As to claim 8, Jeddeloh discloses a processing system, comprising: a processor (614); a memory (628) coupled to said processor for storing program instructions and data values (paragraph 24, lines 55-11 and paragraph 39); multiple device controllers (520 and 524 within DRAM devices 104) coupled to said processor (via 632 through system controller 620; paragraph 39); a plurality of groups of controlled devices (DRAM devices 104 within modules 504 and 508), each group coupled to an associated one of said device controllers (paragraphs 23, 36 and 39), wherein said controlled devices have multiple power management states (Jeddeloh discloses a memory system wherein memory modules can be placed into a power saving mode, can be throttled or use another reduced power mode and thus has multiple power states; paragraph 15, lines 15-20), and wherein said device controllers each include a command unit for sending commands to said associated devices, whereby said devices are power managed by said associated controller (Jeddeloh discloses the controllers managing power to the entire memory module or individually to the DRAM devices; paragraph 24), comprising a sum (average temperature level) of said maximum local bounds (temperature thresholds of the individual DRAM devices 104) (paragraphs 28 and 29), wherein said device controllers include control logic for determining power management states for each device within said associated group of devices consistent with said associated maximum local bound (paragraph 29), whereby said global power consumption bound ("average temperature level across the memory array"; paragraph 28) is met by all of said maximum local bounds (Jeddeloh discloses an average

[global] temperature of the memory devices [104] being maintained based upon individual local thresholds; paragraphs 28 and 29), and wherein said device controller further comprises a command unit for setting said determined power management state of each associated device (Jeddeloh discloses the power controllers [360 or 520 and 524] determining and setting the power states; paragraphs 23 and 29).

Jeddeloh fails to teach: the program instructions stated above also used for determining an associated maximum local bound of power consumption for each of a plurality of groups of devices within said processing system and the total of the local maximum bounds is less than a global maximum power consumption bound for said processing system; communicating each associated maximum local bound to an associated one of a plurality of local controllers coupled to said associated group of devices; and, whereby said global power consumption bound is met by meeting all of said maximum local bounds.

Fung teaches a server rack (52) comprising one or two device controllers (management modules 53) that control and manage the power of multiple groups of devices (server modules 54) (paragraphs 40 and 43). Power management is inclusive of observing server module activity indicators and altering the power states if thresholds within the system are crossed both globally and locally (paragraphs 106-108) wherein said thresholds can be predetermined and set or dynamically (paragraphs 168 and 248) and said thresholds (bounds) are communicated to an associated local controller coupled to said associated group of devices (Fung discloses new activity indicators generated are communicated to the memory of the server modules for use by the activity monitor; paragraph 104). Fung also has the added benefit of managing the overall computer system temperature using cooling fans (paragraph 42).

It would have been obvious to one of ordinary skill of the art having the teachings of Jeddeloh and Fung at the time the invention was made, to modify the device controllers of Jeddeloh to include the ability to dynamically alter activity thresholds as taught by Fung such that the power management scheme of Jeddeloh has the ability to alter thresholds dynamically and communicate new thresholds to the device controllers. One of ordinary skill in the art would be motivated to make this combination of having the ability to alter thresholds dynamically and communicate new thresholds to the device controllers in view of the teachings of Fung, as doing so would give the added benefit of managing the overall computer system temperature using cooling fans (paragraph 42).

Adachi teaches method and apparatus for power saving using clock throttling within an integrated circuit (201) using a device controller (controlled clock generator 202) that collects activity information of a plurality (205, 207 and 209) of groups of devices (functional blocks unit0, unit1, unit2, unit3, unit4, unit5 and unit6) (column 3, lines 43-55) and alters the clock of said devices (column 2, lines 35-4) such that the total of the local bounds (thresholds) is less than a global power consumption bound (measure of global activity) for said processing system (Adachi teaches an activity monitoring technique wherein the sum of the local activity indicators are less than a global threshold such that the total of the local indicators is capable of exceeding the global level; column 9, lines 35-56). Adachi has the added benefit of providing a safe clock throttling technique to that prevents current spikes within the system (column 2, lines 21-34).

It would have been obvious to one of ordinary skill of the art having the teachings of Jeddeloh, Fung and Adachi at the time the invention was made, to modify threshold mechanisms of Jeddeloh to include the sums of the local threshold indicators is less than a global threshold as

taught by Adachi. One of ordinary skill in the art would be motivated to make this combination of ensuring that the global threshold is less than the sum of local threshold in view of the teachings of Adachi, as doing so would give the added benefit of providing a safe clock throttling technique to that prevents current spikes within the system (column 2, lines 21-34).

As to claim 9, Jeddeloh discloses the processing system wherein said device controllers are memory controllers (360), said devices are memory modules (104), and wherein said command unit sets a power management state of each associated memory module (Though Jeddeloh discloses the controllers are within the memory modules and the devices are arrays of DRAM memory it would be known in the art that the same scope can be applied to memory modules and memory controllers; paragraphs 23-24 and 28-29).

As to claim 10, Jeddeloh discloses the processing system wherein said device controllers further comprise evaluators for evaluating a usage of each associated device in order to determine whether or not said usage of each device has fallen below a threshold, and wherein said control logic further determines said power management settings for each particular device in conformity with said measured usage for each particular device (paragraphs 23-24 and 28-29).

As to claim 11, Jeddeloh discloses the processing system wherein said device controllers further include a storage containing an access queue for each of said associated devices, and wherein said control logic further determines said power management settings for each particular device in conformity with a number of accesses queued for each particular device (Jeddeloh discloses responding to a reduction in response time in a memory module dependent on the number commands received which, as is known in the art, is received within a buffer in the system; paragraph 14).

As to claim 12, Jeddeloh discloses the processing system wherein said processing system includes multiple processing locales (104), wherein each of said device controllers is a power management controller for an associated processing locale, whereby said control logic determines the power consumption of each of said multiple processing locales in accordance with meeting said global maximum power consumption bound (paragraphs 28 and 29).

As to claim 13, Jeddeloh discloses the processing system wherein said control sets power management states of said processing locales (104) including a shutdown state of said processing locales (paragraphs 23-24 and 28-29).

As to claim 14, Jeddeloh discloses the processing system wherein said control logic comprises a processor (614) for executing local program instructions (as is known in the art) and memory (628) for storing said local program instructions (paragraph 24, lines 55-11 and paragraph 39), and wherein said local program instructions comprise program instructions for determining power management states for each device within said associated group of devices consistent with said associated maximum local bound, whereby said global power consumption bound is met by meeting all of said maximum local bounds (paragraphs 23-24 and 28-29).

As to claim 15, Fung teaches the processing system wherein said program instructions further comprise program instructions for communicating an associated minimum local bound to an associated one of a plurality of local controllers coupled to said associated group of devices (paragraphs 104, 168 and 248).

Jeddeloh discloses the processing system wherein said control logic further determines said power management states for each device within said associated group of devices consistent with said associated minimum local bound, whereby changes in power consumption of each of

said groups is limited to avoid excessive current spikes within a power distribution network of said processing system (Jeddeloh discloses activity indicators reaching a certain threshold and falling below a certain threshold; paragraphs 23-24 and 28-29).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Sugent whose telephone number is (571) 272-5726. The examiner can normally be reached on 8AM - 4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at (866) 217-9197 (toll-free).

James Sugent
Patent Examiner, Art Unit 2116
April 12, 2006

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